**FAIRCHILD**

SEMICONDUCTOR ™

FDN357N
N-Channel Logic Level Enhancement Mode Field Effect Transistor

General Description

SuperSOT™-3 N-Channel logic level enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage applications in notebook computers, portable phones, PCMCIA cards, and other battery powered circuits where fast switching, and low in-line power loss are needed in a very small outline surface mount package.

Features

- 1.9 A, 30 V, $R_{DS(ON)}$ = 0.090 Ω @ V_{GS} = 4.5 V
  $R_{DS(ON)}$ = 0.060 Ω @ V_{GS} = 10 V.

- Industry standard outline SOT-23 surface mount package using proprietary SuperSOT™-3 design for superior thermal and electrical capabilities.

- High density cell design for extremely low $R_{DS(ON)}$.

- Exceptional on-resistance and maximum DC current capability.

SOT-23	SuperSOT™-6	SuperSOT™-8	SO-8	SOT-223	SOIC-16

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SuperSOT™-3

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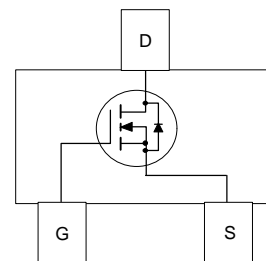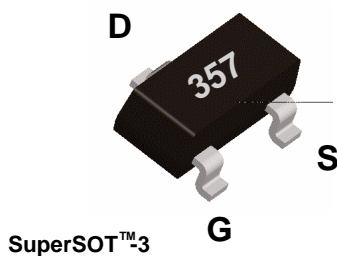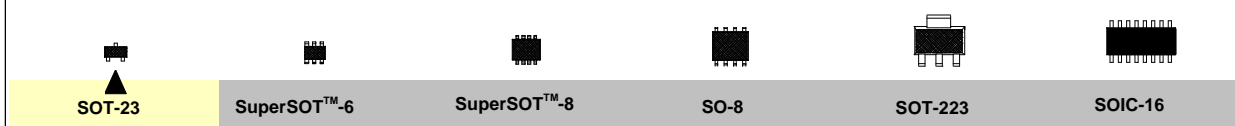
Absolute Maximum Ratings T_A = 25°C unless other wise noted

Symbol	Parameter	FDN357N	Units
V_{DSS}	Drain-Source Voltage	30	V
V_{GSS}	Gate-Source Voltage - Continuous	±20	V
I_D	Drain/Output Current - Continuous	1.9	A
	- Pulsed	10	
P_D	Maximum Power Dissipation (Note 1a)	0.5	W
	(Note 1b)	0.46	
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to 150	°C
THERMAL CHARACTERISTICS			
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	250	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	75	°C/W

Electrical Characteristics (T_A = 25 $^{\circ}$C unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
OFF CHARACTERISTICS							
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA		30			V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	I_D = 250 μA, Referenced to 25 $^{\circ}$C			36		mV/ $^{\circ}$C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V				1	μA
			T_J = 55°C			10	μA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V,V_{DS} = 0 V				100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V				-100	nA
ON CHARACTERISTICS (Note)							
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA		1	1.6	2	V
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Temp. Coefficient	I_D = 250 μA, Referenced to 25 $^{\circ}$C			-3.6		mV/ $^{\circ}$C
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 4.5 V, I_D = 1.9 A			0.081	0.09	Ω
			T_J =125°C		0.11	0.14	
		V_{GS} = 10 V, I_D = 2.2 A			0.053	0.06	
$I_{D(ON)}$	On-State Drain Current	V_{GS} = 4.5 V, V_{DS} = 5 V		5			A
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 1.9 A			5		S
DYNAMIC CHARACTERISTICS							
C_{iss}	Input Capacitance	V_{DS} = 10 V, V_{GS} = 0 V, f = 1.0 MHz			235		pF
C_{oss}	Output Capacitance				145		pF
C_{rss}	Reverse Transfer Capacitance				50		pF
SWITCHING CHARACTERISTICS (Note)							
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = 10 V, I_D = 1 A, V_{GS} = 10 V, R_{GEN} = 6 Ω			5	10	ns
t_r	Turn - On Rise Time				12	22	ns
$t_{D(off)}$	Turn - Off Delay Time				12	22	ns
t_f	Turn - Off Fall Time				3	8	ns
Q_g	Total Gate Charge	V_{DS} = 10 V, I_D = 1.9 A, V_{GS} = 5 V			4.2	5.9	nC
Q_{gs}	Gate-Source Charge				1.3		nC
Q_{gd}	Gate-Drain Charge				1.7		nC
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS							
I_S	Maximum Continuous Drain-Source Diode Forward Current					0.42	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 0.42 A (Note)			0.71	1.2	V

Note:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the   drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

Typical $R_{\theta JA}$ using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment :

a. 250°C/W when mounted on
a 0.02 in^2 pad of 2oz Cu.

b. 270°C/W when mounted on
a 0.001 in^2 pad of 2oz Cu.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width $\leq$ 300μs, Duty Cycle $\leq$ 2.0%.
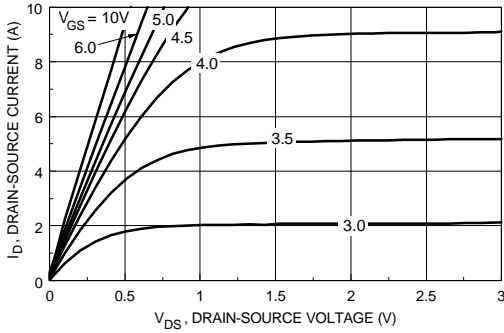
Typical Electrical Characteristics

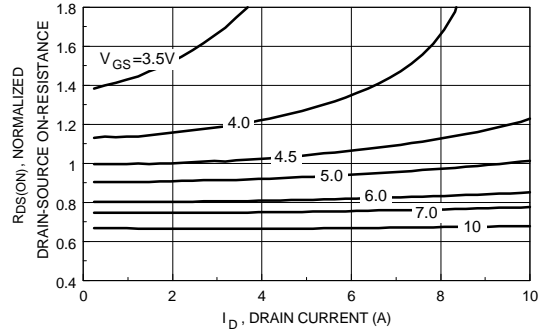Figure 1. On-Region Characteristics.

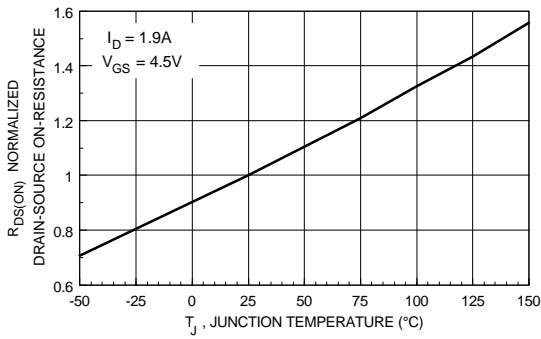Figure 2. On-Resistance Variation with Drain Current and Gate

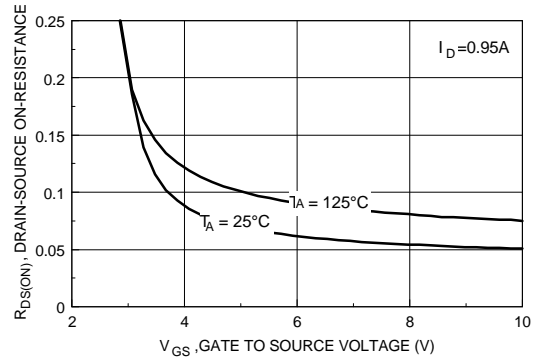Figure 3. On-Resistance Variation with Temperature.

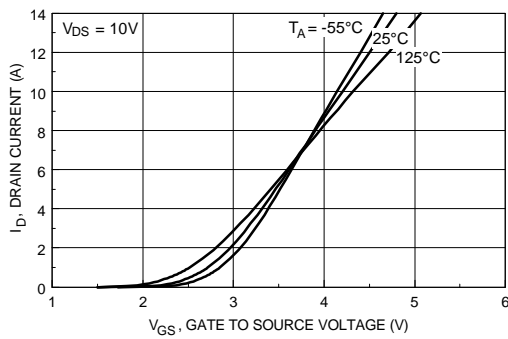Figure 4. On-Resistance Variation with Gate-to-Source Voltage.
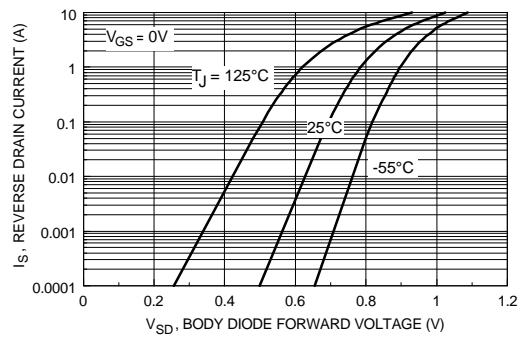

Figure 5. Transfer Characteristics.

Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.
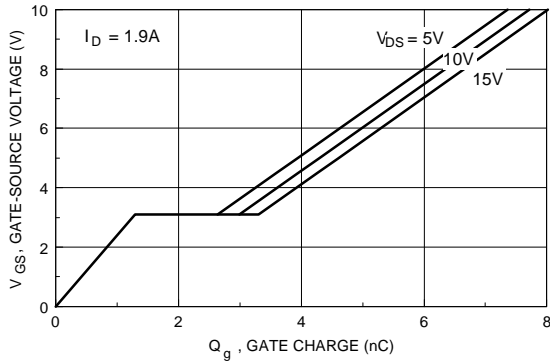
Typical Electrical And Thermal Characteristics

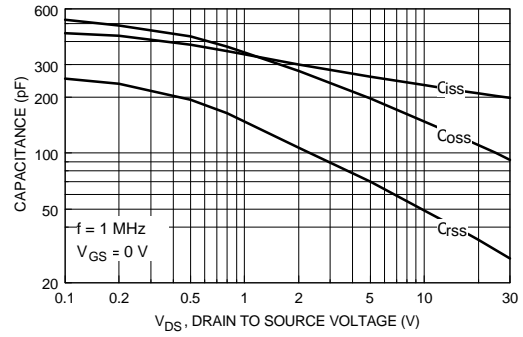**Figure 7. Gate Charge Characteristics.**

X-axis: Q_g, GATE CHARGE (nC)
Y-axis: V_{GS}, GATE-SOURCE VOLTAGE (V)
$I_D = 1.9A$
$V_{DS} = 5V$, 10V, 15V

Figure 8. Capacitance Characteristics.

X-axis: V_{DS}, DRAIN TO SOURCE VOLTAGE (V)
Y-axis: CAPACITANCE (pF)
Ciss, Coss, Crss
f = 1 MHz
$V_{GS} = 0 V$
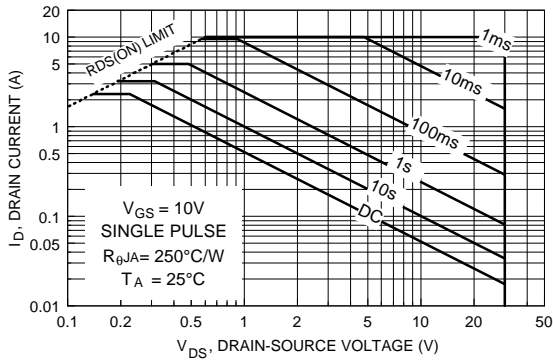
Figure 9. Maximum Safe Operating Area.

X-axis: V_{DS}, DRAIN-SOURCE VOLTAGE (V)
Y-axis: I_D, DRAIN CURRENT (A)
RDS(ON) LIMIT
1ms, 10ms, 100ms, 1s, 10s, DC
$V_{GS} = 10V$
SINGLE PULSE
$R_{\theta JA} = 250°C/W$
$T_A = 25°C$
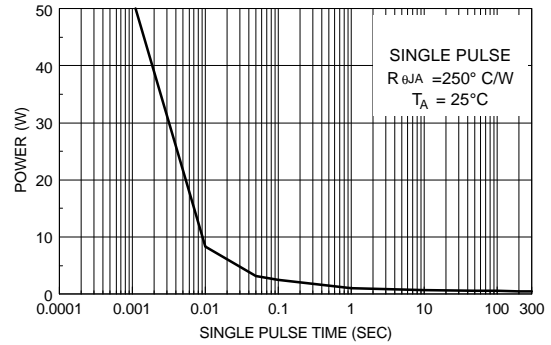
Figure 10. Single Pulse Maximum Power Dissipation.

X-axis: SINGLE PULSE TIME (SEC)
Y-axis: POWER (W)
SINGLE PULSE
$R_{\theta JA} = 250° C/W$
$T_A = 25°C$
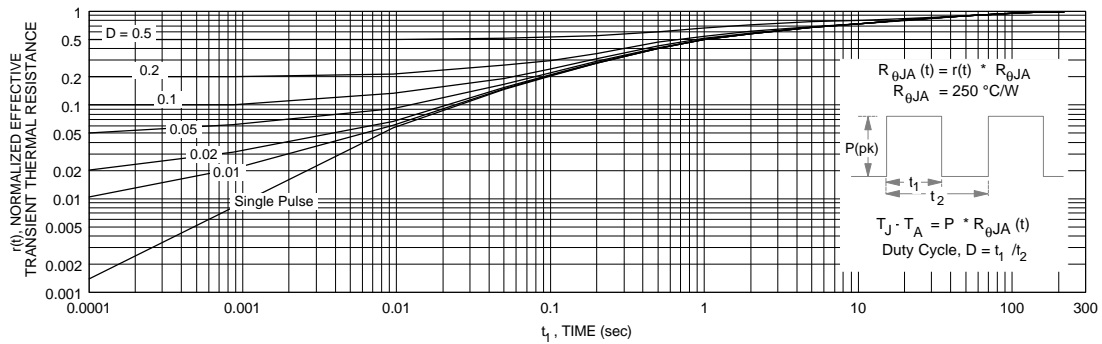
Figure 11. Transient Thermal Response Curve.

X-axis: t_1, TIME (sec)
Y-axis: r(t), NORMALIZED EFFECTIVE TRANSIENT THERMAL RESISTANCE
D = 0.5, 0.2, 0.1, 0.05, 0.02, 0.01
Single Pulse
$R_{\theta JA} (t) = r(t) * R_{\theta JA}$
$R_{\theta JA} = 250 °C/W$
P(pk)
t_1
t_2
$T_J - T_A = P * R_{\theta JA} (t)$
Duty Cycle, $D = t_1 / t_2$

Note: Thermal characterization performed using the conditions described in note 1a.
Transient thermal response will change depending on the circuit board design.